RFID circuit with read/write functions

The MINI5577 (equivalent of EM4100 EM Microelectronic – Marin SA) is chip for multifunction contactless read/write cards with 64 bit EEPROM
The MINI5577 is intended for application in the RF identification systems. External coil has to be connected to chip to create contactless ID tag. Build-in radio channel receives signal induced in antenna. This signal is used by power supply unit to generate supply voltage & by control unit to separate clocking signal. Data exchange is performed by means of modulation of the carrier frequency
Application areas: access control systems in buildings, restricted areas, industrial RFID tags. Read/write operations of 64 EEPROM is performed via built-in radio channel with the frequency of 100-150 kHz

Main features:

- Contactless data exchange.
- Power supply from the external aerial (coil), placed in the electromagnetic field, (electromagnetic oscillations with the frequency of 125 kHz)
- Internal DC voltage limitation to prevent identifier tag fail in power electromagnetic field
- 64 bit EEPROM.
- data storage without power supply (nonvolatile memory);
- Data transfer by means of amplitude modulation;
- Data transfer ratio RF/64;
- Manchester coding of data.
- 100,000 memory program/erase cycles;
- Temperature range from minus 45 to plus 85 °C;
- ESD protection up to 2000 V;

Table 1 – Contact pad description

Contact pad number	Symbol	Function
01	COIL1	Coil connection I/O
02	COIL2	Coil connection I/O
03	GND	Common
04	U_{CC}	Power supply
Note – Contact pads U_{CC}, GND are purposed only for testing during IC manufacturing and are not used by customer		

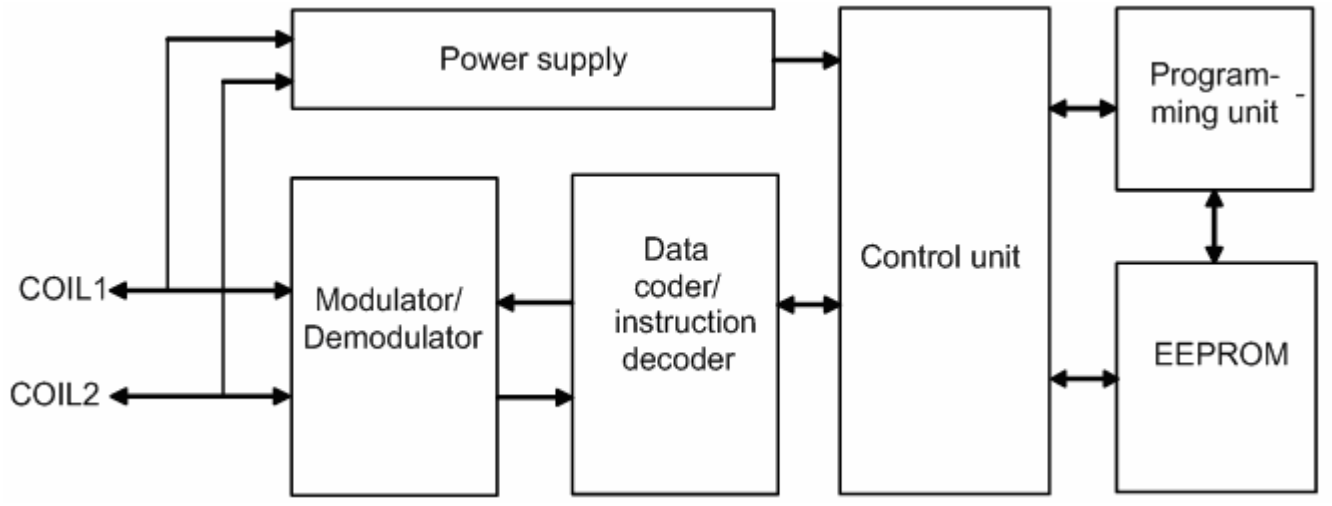


Fig. 1 – Block diagram

Table.2 Maximum ratings

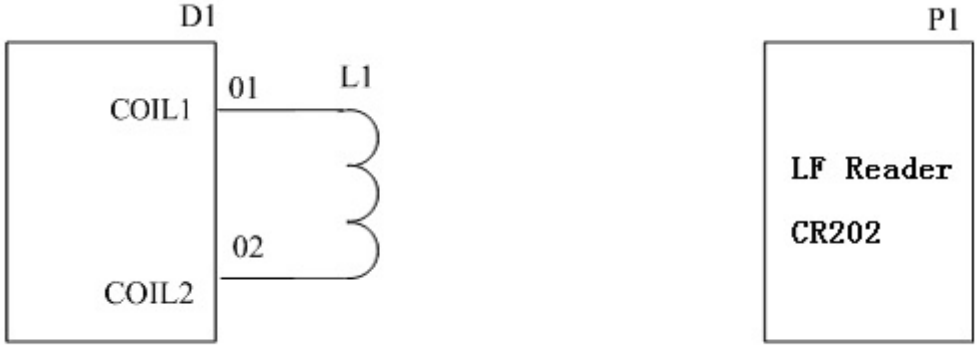
Symbol	Parameter	Target		Unit
		min	max	
I_I	Input current	-	30	mA
T	Ambient temperature	- 60	125	^oC

Table. 3 Recommended operation modes

Symbol	Parameter	Target		Unit
		min	max	
I_I	Input current	–	10	mA
f_{COIL}	Operating frequency	100	150	kHz
T	Operating ambient temperature	- 45	85	^oC

Table. 4 – Electric parameters

Symbol	Parameter	Mode of testing	Value		Ambient temperature, °C	Unit
			min	max		
I_{CC}	Consumption current	U_{CC}= 1,7 V	-	1,45 1,50	25±10 85 -40	uA
C_{RES}	Resonance capacity	f_{COIL} = 125 kHz	460	490		pF
Umod	Output voltage of modulator	U_{CC} = 4,0 V Imod = 1,0 mA	1,65 1,50	2,90 3,00		V
r*	Reading range	f_{COIL} = 125 kHz	8,0 9,0	-		sm
* For readers CR202 refer Fig. 2. inductance coil and aerial of reader have be placed in alignment						

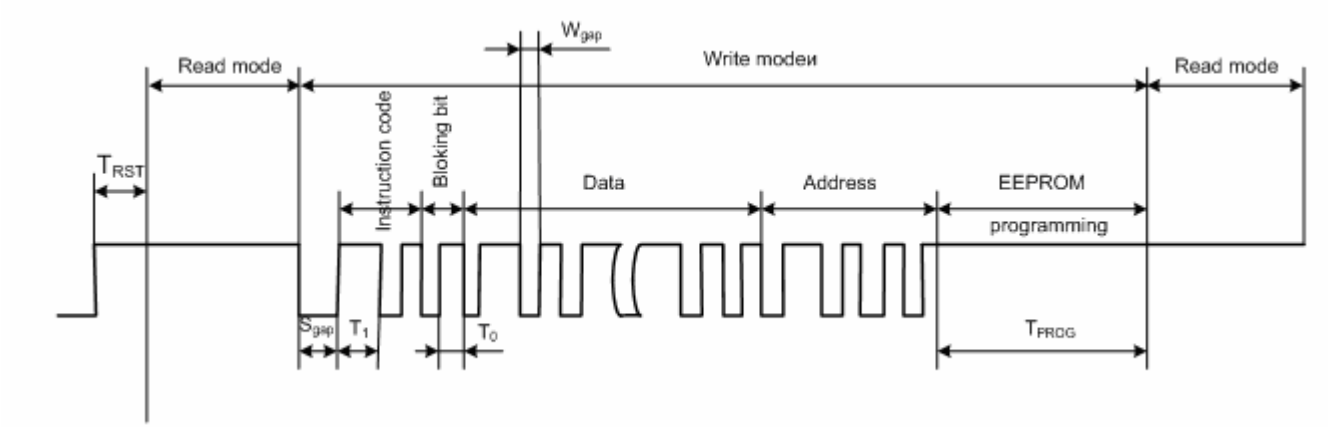


D1 – integrated circuit
L1 – inductance coil 3,38 uH (S = 70 x 42 mm)
P1 – reader 2270 or EM4469 for example CR202 CR208

Fig. 2 – Recommended application

Operation

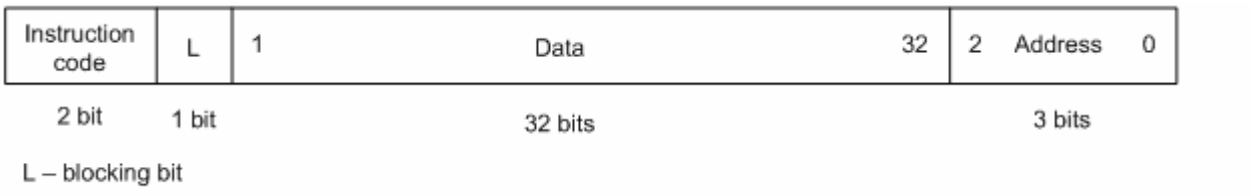
Tag being placed in the field of the reader switches over to READ mode and transmits the EEPROM content continuously. On receiving Write instruction tag switches over to WRITE mode and after Write operation completed returns to Read mode.
Data from the tag to a reader transferred by means of amplitude modulation of carrier frequency. Manchester coding used to represent data bits
Write/read operations of ROM are performed in accordance with the time diagram shown in Figures 3 - 5.



Parameter	Value		Comment
	Min	Max	
t_{RST}	>50 μs	-	Reset time
S_{gap}	10 T_{CLK}	50 T_{CLK}	Start gap
W_{gap}	8 T_{CLK}	30 T_{CLK}	Neighbor bit gap (transmitted)
T_1	48 T_{CLK}	63 T_{CLK}	Pulses number at delivery of '1'
T_0	16 T_{CLK}	31 T_{CLK}	Pulses number at delivery of '0'
T_{PROG}	>2ms	-	EEPROM programming cycle

T_{CLK} (T_{OC}) - one clock cycle 125 kHz

Fig 3 – Write mode timing diagramm



At write operation most significant bit follows fist (high-order bit – left bit).
Instruction code: 10
L- memory lock bit («1» - 32 bit row is locked).
Once set lock bit to «1» irreversibly disable memory write function.
Address of page:
001 – first page
010 – second page

Fig. 4 – Write instruction format

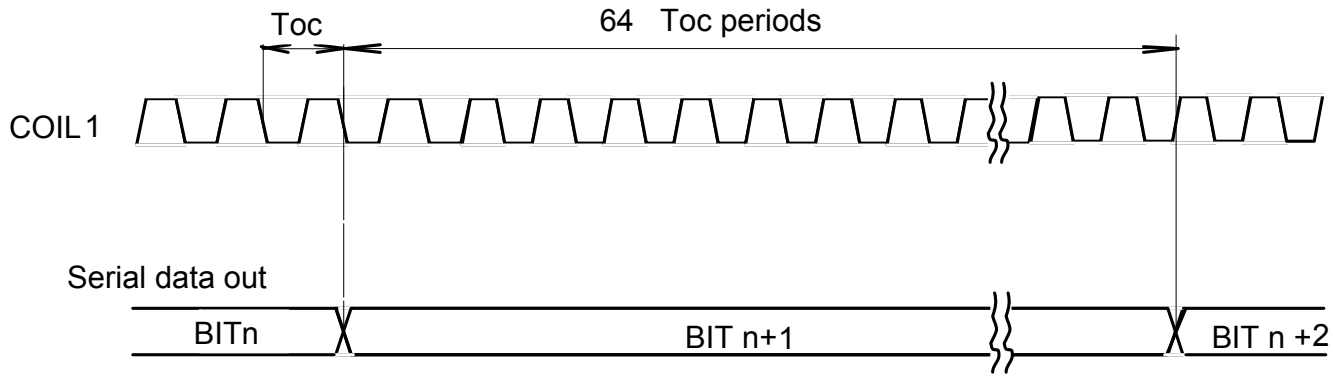


Fig. 5 - Data reading

EM-Marin format code structure

The memory contains 64 bits divided in five groups:
- 9 bits are used for the header, ROM area (“111111111”);
- 10 row parity bits (P0-P9);
- 4 column parity bits (PC0-PC3);
- 40 data bits (D00-D93);
- 1 stop bit set to logic 0.

The header is composed of the 9 first bits which are all programmed to "1".
The header is followed by 10 data rows each consist of 4 data bits and 1 row parity bit. The last row consists of 4 column parity bits and 1 stop-bit S0 which is written to "0".
Row parity bit is set to "0" if row contain even number of bits programmed to “1”. otherwise row parity bit is set to "1", so data array is arrange in such way that dataflow never contain more than 4 “1”-bits (except header)
The exception - 9 bits of header programmed to "1" divides continuous dataflow to 64 bits units and serves to organize the synchronization with the reader.
Bits D_{00}-D_{03}, D_{10}-D_{13} (8 bits) define version and customer identification code. The rest of bits D_{20}-D_{93} (32 bits) – data bits, define «unique code» of chip.
Structure of code under EM-Marin format is shown at Fig. 6.

Header				00…08	(Cell number)
				“111111111”	(Cell state)
Customer code	09	10	11	12	13
	D_{00} (Cell address)	D_{01}	D_{02}	D_{03}	$P_0 = D_{00}\text{^}D_{01}\text{^}D_{02}\text{^}D_{03}$
	14	15	16	17	18
	D_{10}	D_{11}	D_{12}	D_{13}	$P_1 = D_{10}\text{^}D_{11}\text{^}D_{12}\text{^}D_{13}$
Unique code (number) of the chip	19	20	21	22	23
	D_{20}	D_{21}	D_{22}	D_{23}	$P_2 = D_{20}\text{^}D_{21}\text{^}D_{22}\text{^}D_{23}$
	24	25	26	27	28
	D_{30}	D_{31}	D_{32}	D_{33}	$P_3 = D_{30}\text{^}D_{31}\text{^}D_{32}\text{^}D_{33}$
	29	30	31	32	33
	D_{40}	D_{41}	D_{42}	D_{43}	$P_4 = D_{40}\text{^}D_{41}\text{^}D_{42}\text{^}D_{43}$
	34	35	36	37	38
	D_{50}	D_{51}	D_{52}	D_{53}	$P_5 = D_{50}\text{^}D_{51}\text{^}D_{52}\text{^}D_{53}$
	39	40	41	42	43
	D_{60}	D_{61}	D_{62}	D_{63}	$P_6 = D_{60}\text{^}D_{61}\text{^}D_{62}\text{^}D_{63}$
	44	45	46	47	48
	D_{70}	D_{71}	D_{72}	D_{73}	$P_7 = D_{70}\text{^}D_{71}\text{^}D_{72}\text{^}D_{73}$
	49	50	51	52	53
	D_{80}	D_{81}	D_{82}	D_{83}	$P_8 = D_{80}\text{^}D_{81}\text{^}D_{82}\text{^}D_{83}$
	54	55	56	57	58
	D_{90}	D_{91}	D_{92}	D_{93}	$P_9 = D_{90}\text{^}D_{91}\text{^}D_{92}\text{^}D_{93}$
Column parity control	59	60	61	62	63
	$PC_0 = D_{00}\text{^}D_{10}\text{^}\text{^}D_{20}\text{^}D_{30}\text{^}D_{40}\text{^}\text{^}D_{50}\text{^}D_{60}\text{^}\text{^}D_{70}\text{^}D_{80}\text{^}D_{90}$	$PC_1 = D_{01}\text{^}D_{11}\text{^}\text{^}D_{21}\text{^}D_{31}\text{^}D_{41}\text{^}\text{^}D_{51}\text{^}D_{61}\text{^}\text{^}D_{71}\text{^}D_{81}\text{^}D_{91}$	$PC_2 = D_{02}\text{^}D_{12}\text{^}\text{^}D_{22}\text{^}D_{32}\text{^}D_{42}\text{^}\text{^}D_{52}\text{^}D_{62}\text{^}\text{^}D_{72}\text{^}D_{82}\text{^}D_{92}$	$PC_3 = D_{03}\text{^}D_{13}\text{^}\text{^}D_{23}\text{^}D_{33}\text{^}D_{43}\text{^}\text{^}D_{53}\text{^}D_{63}\text{^}\text{^}D_{73}\text{^}D_{83}\text{^}D_{93}$	S0 = 0

Row parity control

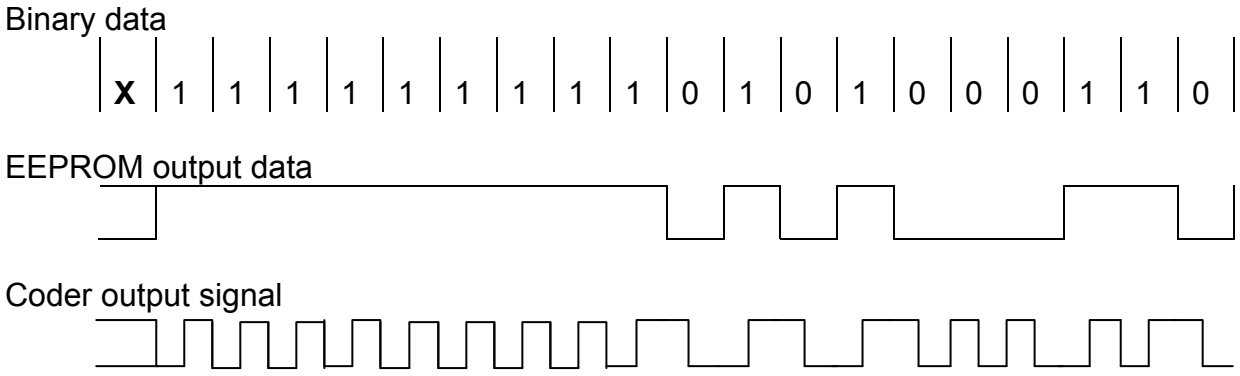
Stop bit

Note - **^** - «XOR» logic operation

Fig 6 – Structure of data memory

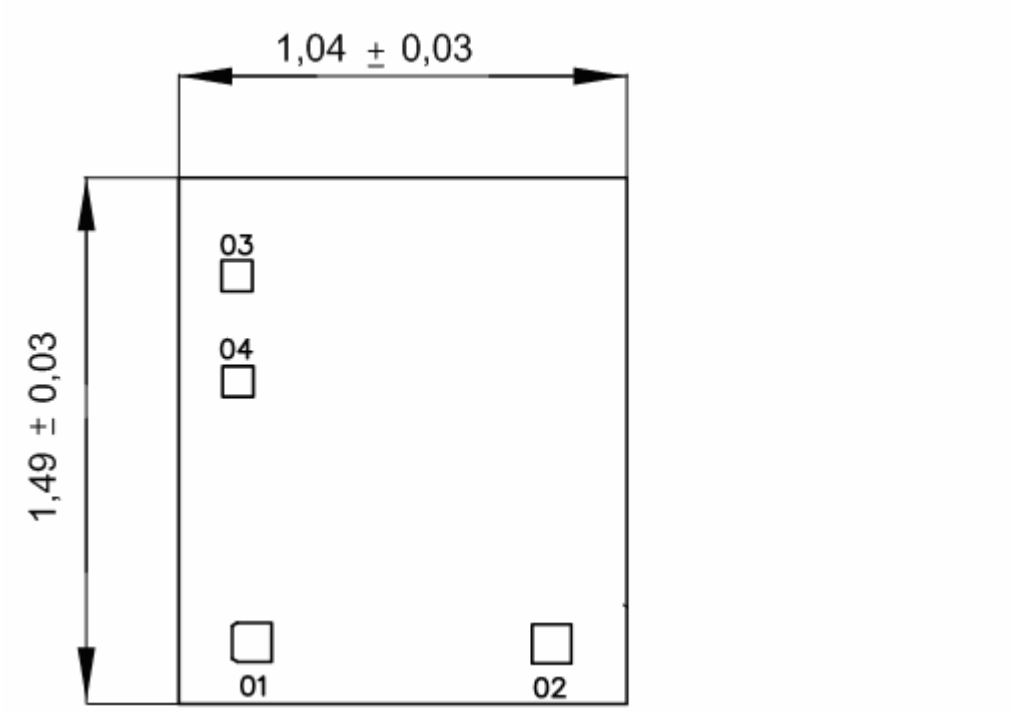
Manchester code

At Manchester data coding there is a transition in the middle of each bit period from from LOW to HIGH (logic bit “1” is transmitted) or from HIGH to LOW (logic bit “0” is transmitted). (see Fig. 7).



«1» – High level voltage
«0» – Low level voltage
«X» – Don’ care (low or high level voltage)

Fig. 7 Manchester code



Technological mark coordinates (mm): left bottom corner x = 0,790, y =0,248.
Die thickness 0,46±0,02 mm.

Contact pad number	Coordinates (Left bottom corner), mm		Contact pad dimensions, mm
	X	Y	
01	0,229	0,127	0,092 x 0,092
02	0,719	0,127	0,092 x 0,092
03	0,114	1,225	0,072 x 0,072
04	0,116	0,922	0,072 x 0,072
Note: Contact pad coordinates and size are indicated under «Passivation» layer			

Fig. 8 – Chip diagram and contact pad location