CMOS IC FOR ELECTRONIC KEY

DESCRIPTION

CMOS microcircuit is essentially an electronic carrier of the unique 64-bit digital code. The code is stored in the internal nonvolatile memory. The data exchange is performed by the protocol 1-Wire, which requires one sole data pin and the common pin. The microcircuit supports the function of the protocol 1-Wire of ROM search, which makes it possible for several devices to operate on one bus. This protocol determines the alteration conditions of the bus status and the time intervals during synchronization by the synchropulses cuts of the control device. Data read-out and writing are performed by the junior significant bit forward.

TRANSACTION SEQUENCE

Access sequence to SW-1990/2 via 1-Wire port is as follows:

- Initialization
- ROM function command
- Data read-out

INITIALIZATION

All transactions on the bus 1-Wire start with the initialization sequence. The initialization sequence consists of the reset pulse, applied by the bus master, followed by the availability pulse (or pulses), applied by the slave buses (or slave buses).

The availability pulse informs the bus master, that SW-1990 is connected to the bus and is ready for operation.

ROM FUNCTIONS COMMANDS

After the bus master has determined availability of the device, it can apply one out of four commands for operation with ROM. All commands for operation with ROM have the length of 8 bits. These commands are enumerated below (see also the diagram in Fig. 4)

ROM Reading [33h] or [0Fh]

This command enables bus master to read the 8-bit group code SW-1990/2, its unique 48-bit serial number and 8-bit CRC. This command can be used only, if the bus has one device SW-1990/2. If the bus has more, than one slave, there will be a conflict of data, when all slave ones, when all slave ones attempt to apply at the same time (the open drains will apply the mount AND). In SW-1990/2 the function ROM Reading may work with the command byte 33h or 0Fh, which ensures compatibility with the devices **DS1990**, which will respond only to the command word 0Fh.

Comparison of ROM [55h] / ROM Skipping [CCh]

As the device SW-1990/2 contains only 64-bit ROM, the commands COMPARISON OF ROM and ROM SKIPPING from Protocol 1-Wire are not applied and do not case the response on the bus, if applied by the master.

Search of ROM [F0h]

When the system is started initially, the bus master may not know the numbers of the devices, connected to the bus 1-Wire or their 64-bit ROM codes. The ROM search command enables the bus master to use the exception process, in order to determine the 64-bit ROM codes of all slave devices on the bus. The ROM search process is essentially repetition of a simple procedure, consisting of three steps: bit reading, reading bit by bit supplement, and then writing of the required value of the given bit. The bus master performs this simple step procedure by each ROM bit. After completion of one entire run the bus master knows the ROM contents of one device. Numbers of the remaining devices and the codes of their ROMs can be determined by means of the additional runs.

SIGNALIZATION OF BUS 1-WIRE

In order to ensure integrity of data, the device SW-1990/2 requires the strict observance of the protocols. The protocol consists of the four types of signalization on one line: sequence of resetting with the reset pulse and availability pulse, low writing, high writing and data read-out. With exception of the availability pulse, all these signals are initialed by the master. The initialization sequence, required for start of any informational exchange with SW-1990/2 is indicated in Figure 1. After the reset pulse follows the availability pulse, which indicates, that the device SW-1990/2 is ready for reception of the ROM command. The bus master applies the reset pulse (t_{RSTL}, minimum 480 usec). Then the bus master vacates (releases) the line and switches over to the reception mode. Bus 1-Wire is pulled up to the status of the HIGH level via the pull-up resistor. After detection of the rising front at the data pin the device SW-1990/2 is in the stand-by mode (t_{PDH}, from 15 to 60 usec), and then applies the availability pulse (t_{PDL}, from 60 to 240 usec).

INITIALIZATION PROCEDURE. RESET AND AVAILABILITY PULSES

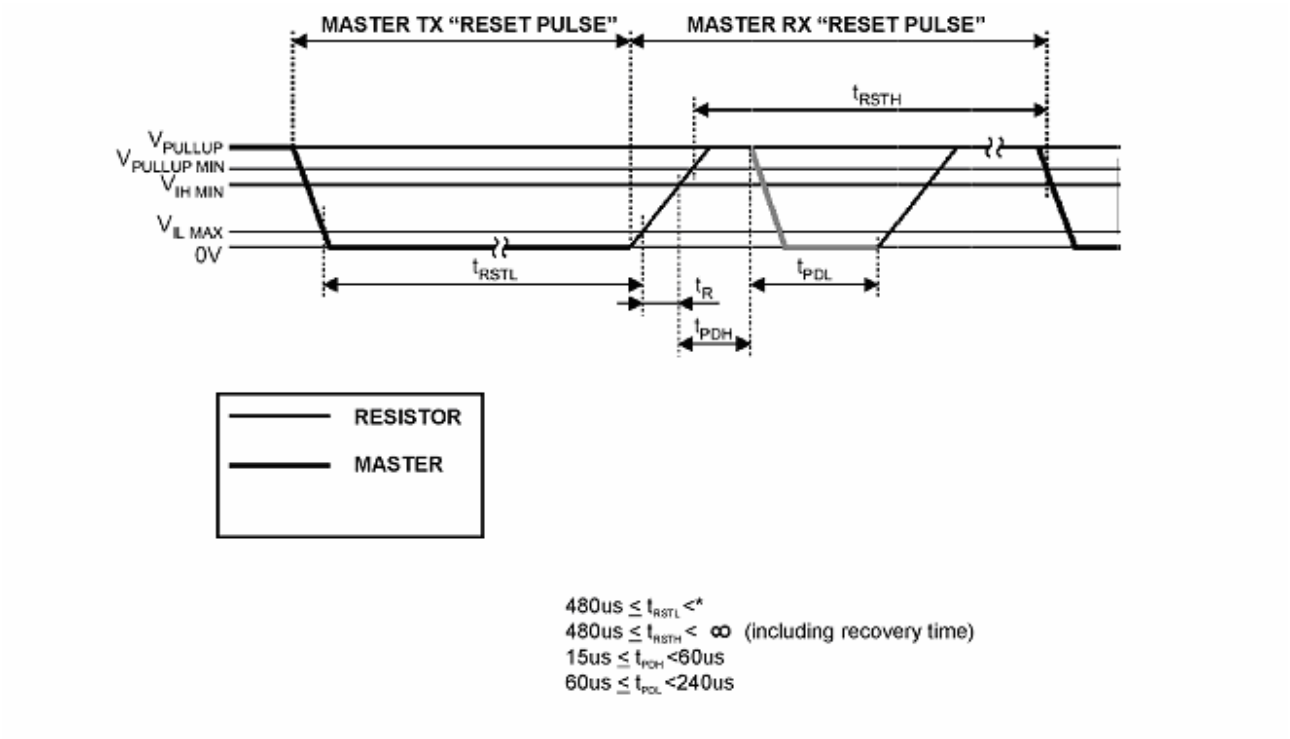


Figure 1. – Initialization of the device SW-1990/2

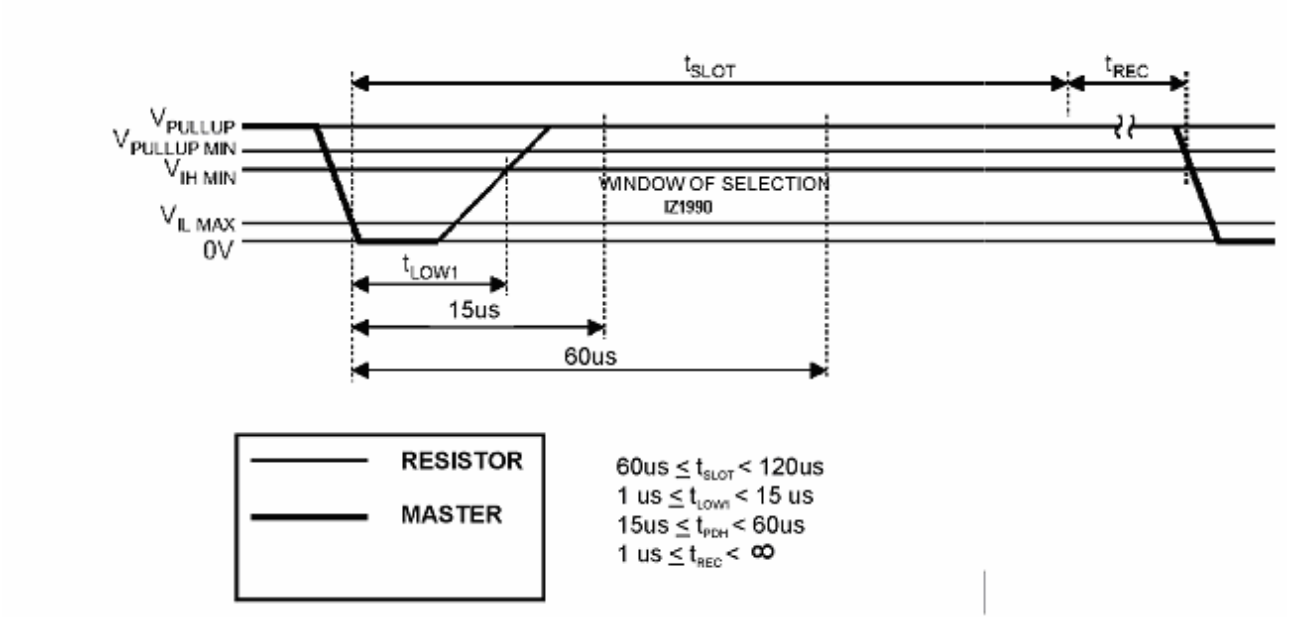
In order so as not to mask the interruption signals, applied from the other devices on the bus 1-Wire, the interval t_{RSTL} + t_R should always be less, than 960 usec.

TIME INTERVALS OF READ-OUT / WRITING

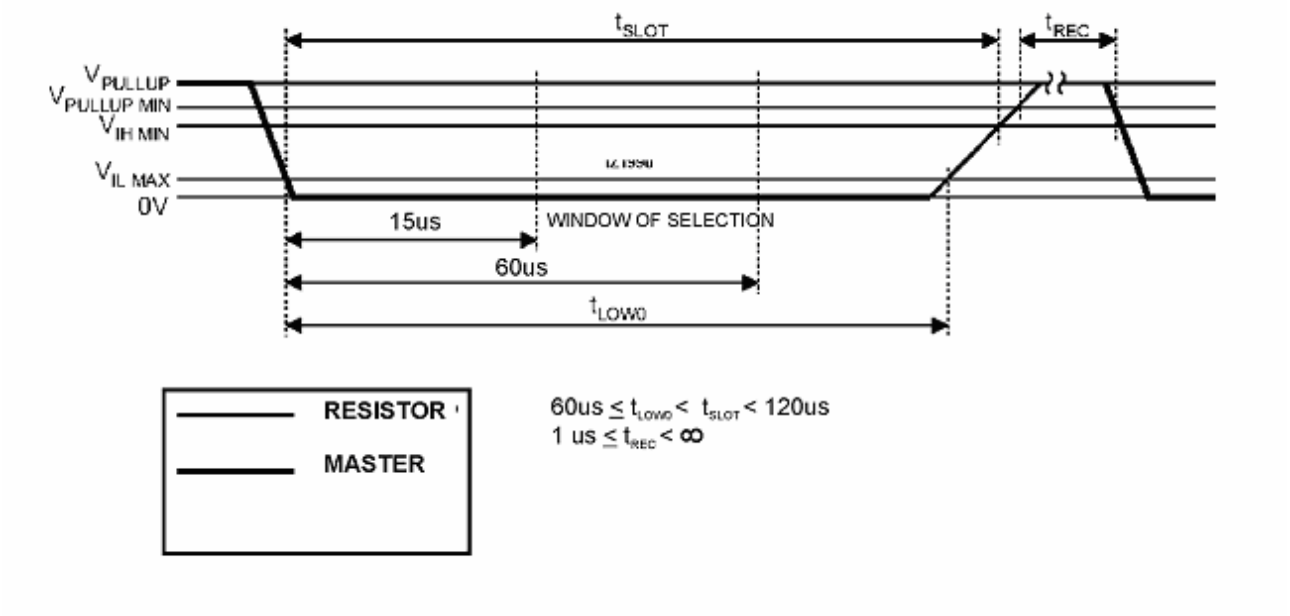
Determinations of the time intervals for writing and read-out are illustrated in Figure 2. All time intervals are initiated by the master, which transfers the data line to the LOW level. The falling front on the data line synchronizes SW-1990/2 with the master, starting the delay time in SW-1990/2. During the write time the delay circuit determines, when SW-1990/2 will perform selection on the data line. For the time interval of the data read-out, if 0 is applied, the delay circuit determines, how long SW-1990/2 will hold the data line on the LOW level, interlocking 1, generated by the master. If the data bit is equal to 1, SW-1990/2 will leave the time interval of the data read-out unaltered.

TIME CHART OF READ-OUT / WRITING

Writing 1



Writing 0



Read-out

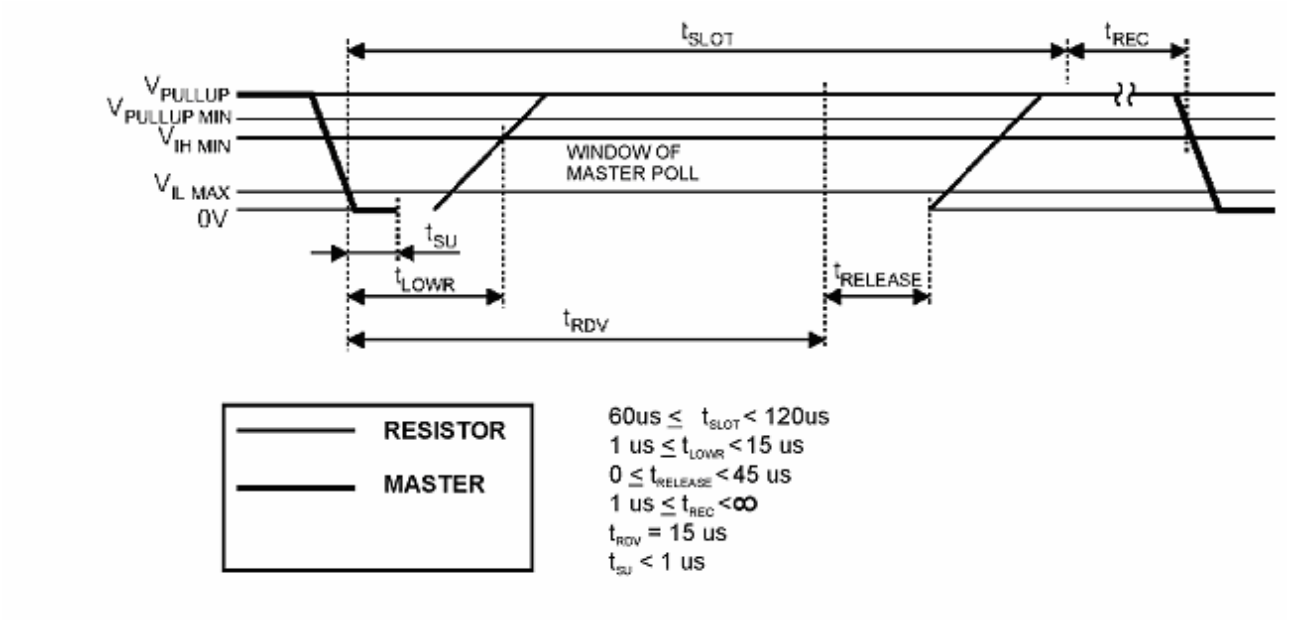


Figure 2 – Procedures of writing / read-out

EQUIVALENT CIRCUIT SW-1990/W

Equivalent circuit 1-Wire of port IC SW-1990/2 is listed in Figure 3.

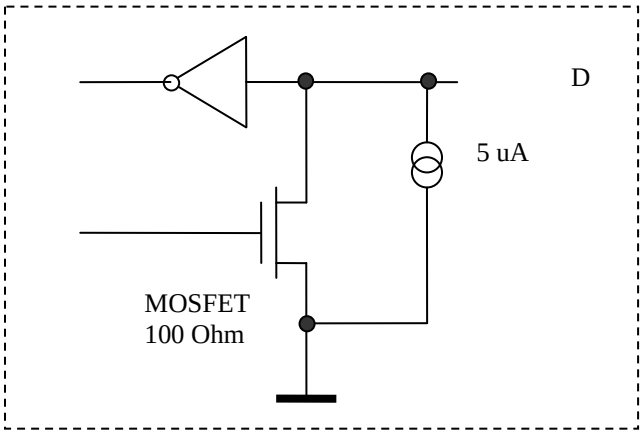


Figure 3 - Equivalent circuit 1-Wire of port SW-1990/2.

LIMIT MODE

PARAMETER	IDENTIFICATION	VALUE	MEASUREMENT UNIT
Voltage at pins relative to GND		- 0.5 ÷ + 7.0	V
Operating temperature	T_{por}	- 40 ÷ + 85	^{o}C
Limit temperature	T_{stg}	- 55 ÷ + 125	^{o}C

ELECTRIC PARAMETERS (* Vpup = 2.8 ÷ 6.0 B, T =-40 ÷ +85)

Parameter	Identifi-cation	Measurement Mode	Min.	Type	Max.	Measure-ment Units
Input voltage of logic “1”	V_{IH}		2.2		Vpup+0.3	V
Input voltage of logic “0”	V_{IL}		-0.3		+0.8	V
Low level output voltage	V_{OL}	I_{OUT} = 4 mA			0.4	V
High level output voltage	V_{OH}			Vpup	6.0	V

- Vpup *–voltage level on the external pull-up resistor.*

DYNAMIC PARAMETERS (* Vpup = 2.8 ÷ 6.0 V, T =-40 ÷ +85)

Parameter Description, Measurement Unit	Identification	Min.	Type	Max.	Measure-ment Unit
Duration of time interval	t_{SLOT}	60		120	usec
Low level duration in writing 1	t_{LOW1}	1		15	usec
Low level duration in writing 0	t_{LOW0}	60		120	usec
Interval of valid data in read-out	t_{RDV}	15			usec
Time for vacating the bus	$t_{RELEASE}$	0	15	45	usec
Time for presetting data for read-out	t_{SU}			1	usec
Restoration time	t_{REC}	1			usec
High level duration in reset	t_{RSTH}	480			usec
Low level in reset	t_{RSTL}	480			usec
High level of availability pulse	t_{PDH}	15		60	usec
Low level of availability pulse	t_{PDL}	60		240	usec